96767760
B

CONTROL DATA CORPORATION

CDC® CHANGE OF STATE UNIT

DK617-A

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE MAINTENANCE MANUAL

96767760

CONTROL DATA CORPORATION

CDC® CHANGE OF STATE UNIT

DK617-A

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released.
(4/76)	
B	Manual revised; includes ECO DS18803, re-identifying QSE 18340 as equipment number DK617-A and ECO DS15354,
(3/78)	correcting minor manual errors. The front cover, pages ii, iii, v, vii, ix, 1-1, 2-1, and 3-1, and the comment sheet
	are revised.

Publication No.
96767760

REVISION LETTERS I, O, Q AND X ARE NOT USED

© 1976, 1978
by Control Data Corporation

Printed in the United States of America

Address comments concerning this manual to:

Control Data Corporation
Publications and Graphics Division
4455 Eastgate Mall
La Jolla, California 92037

or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
QSE 18340	01		
DK617-A	01	ECO DS18803	

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

PAGE	REV	PAGE	REV	PAGE	REV	PAGE	REV	PAGE	REV
Cover	--								
Title page	--								
ii	B								
iii/iv	B								
v/vi	B								
vii/viii	B								
ix	B								
1-1	B								
1-2	A								
2-1	B								
2-2	A								
3-1	B								
3-2	A								
4-1	A								
4-2	A								
5-1 thru 5-5	A								
6-1	A								
6-2	A								
7-1 thru 7-3	A								
Comment sheet	B								
Cover	--								

PREFACE

This manual contains the theory of operation, diagrams, and maintenance for the CDC® DK617-A Digital Change of State Unit. The digital change of state unit occupies one station in either the EL101-A Computer Interface Unit or the EL102-A Computer Interface Expander.

This manual is intended for use by customer engineering personnel familiar with the 1750 Computer Interface Unit/Computer Interface Expander.

Other related documents that may be useful to the reader are listed below.

Description	Publication No.
EL101-A Computer Interface Unit/ EL102-A Computer Interface Expander Hardware Reference/Maintenance Manual	88980100
Key to Logic Symbols	88981500
Input/Output Specification Manual	60165800
1700 Computer Reference Manual	60153100

CONTENTS

FIGURES

TABLE

The CDC® Digital Change-of-State Unit (DCOS) monitors 16 digital inputs. The 16-bit input word is read on command from the control computer, and this data is stored in the unit as a reference for determining state changes. Any change in the inputs with respect to the reference data initiates an interrupt to the computer via the computer interface unit (CIU) or the computer interface expander (CIE). Signal conditioning delays are provided on the unit for logic level inputs or for contact closures. The interrupt does not occur until completion of the delay interval. A simplified logic diagram is shown in figure 5-1.

The digital change-of-state unit occupies one station in the computer interface unit or the computer interface expander.

PERFORMANCE/CHARACTERISTICS

PERFORMANCE

- Number of inputs

  16 per card, 256 per computer interface expander/ computer interface unit module, 2048 per equipment number

- Input levels

  Logic levels: Low state, 0v +0.4v
  High state, +2.4v to +5.25v

- Contact closures: Each bit formed from one isolated contact pair. One pole of each pair connects to ground.

- Signal conditioning delays

  Adjustment of the signal conditioning delays is by nut and bolt jumper and potentiometer. The delay time is user-selected to exceed the contact bounce interval anticipated with user's inputs.

  The delays are adjustable from 1.0 milliseconds to 10 milliseconds for use with contact closure inputs. The delay for logic level inputs is adjustable to 1 microsecond.

  The delay intervals initiate at the first bounce of the change of state. The interrupt occurs at the completion of the delay; this prevents the generation of a series of interrupts from contact bounce.

- Interrupt

  Interrupt capability is enabled by function output instruction. A change of state causes the interrupt flag to be activated at completion of the signal conditioning delay interval.

- Addressing capability

  The unit may be installed in any station location of the computer interface unit or computer interface expander.

- Programming considerations

  The unit responds to data input and function output instructions. Data output and status input are not recognized.

RELIABILITY

The estimated mean time between failures is 100,000 hours. The mean time to repair is 0.5 hour. Diagnostics are provided.

ELECTROMAGNETIC INTERFERENCE

The unit is designed in accord with CDC Standard 1.30.020.

EQUIPMENT CONFIGURATION

The change-of-state unit is a single plug-in card that can be inserted into any station in the computer interface unit/computer interface expander, including station 0.

Inputs are by 28-pin I/O connector at the computer interface unit/computer interface expander backplane.

ELECTRICAL REQUIREMENTS

Power: +5v logic power is supplied by the computer interface unit/computer interface expander module power. No special supplies are required.

Size: Single 7-3/4- by 9-inch computer interface unit/computer interface expander plug-in card.

Cooling: Forced air is provided by the peripheral equipment cabinet.

ENVIRONMENTAL REQUIREMENTS

Operating temperature: $40^{\circ}F$ to $120^{\circ}F$

SIGNAL CONDITIONING DELAY JUMPER

The jumper consists of a nylon nut and bolt with one metal washer that electrically connects pairs of printed circuit contacts. The position of the metal washer determines the delay time. The nylon nut and bolt positions the metal washer across the contacts.

ONE MICROSECOND DELAY

The washer is secured at the position marked DELAY A for delays up to one microsecond.

ONE MILLISECOND DELAY

The washer is secured at the position marked DELAY B for delays up to one millisecond.

TEN MILLISECOND DELAY

The washer is secured at the position marked DELAY C for delays up to 10 milliseconds

SIGNAL CONDITIONING DELAY POTENTIOMETER

Potentiometer R4 provides the fine adjustment to delay time for each position of the nut and bolt jumper.

DELAY A

The washer is secured at the position labeled DELAY A for minimum delay. This range is for use with logic level inputs or no-bounce inputs. This interval is adjustable to 1 microsecond.

DELAY B

The washer is secured at the position labeled DELAY B. This delay interval is adjustable to 1 millisecond for use with contact closure inputs.

DELAY C

The washer is secured at the position labeled DELAY C. This delay interval is adjustable to 10 milliseconds for use with contact closure inputs that are prone to extensive bounce.

DELAY ADJUSTMENT POTENTIOMETER

Potentiometer R4 provides a fine adjustment to the delay interval for each position of the nut and bolt jumper.

PROGRAMMING INFORMATION

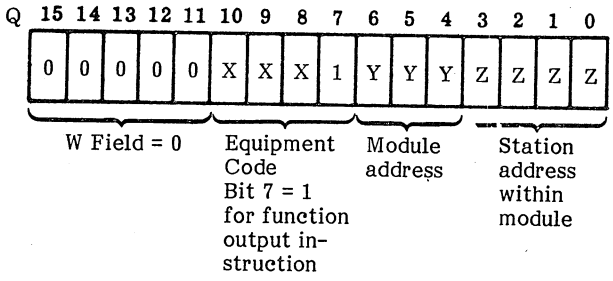
The digital change of state recognizes function output and data input instructions. The computer address must specify the station address of the digital change-of-state location in the computer interface unit/computer interface expander module.

FUNCTION OUTPUT INSTRUCTION (WRITE FUNCTION)

A write function instruction with the A register equal to 0001_{16} enables the interrupt mode of the digital change of state.

A write function instruction with the A register equal to 0000_{16} disables the interrupt mode of the digital change of state. The following Q register format is used for function output:

Address



DATA INPUT INSTRUCTION (READ DATA)

The digital change of state inputs the current field input word to the central processing unit upon receipt of a read data instruction. The input word becomes the updated reference data.

MASTER CLEAR

MASTER CLEAR pressed on the console disables the interrupt mode and resets the delay one-shot.

STATUS INPUT AND DATA OUTPUT INSTRUCTIONS

The digital change of state is always ready; it does not initiate external reject.

Status input or data output instructions result in internal rejects.

INTERRUPT FLAG

A change of state results in the interrupt flag going active, provided the interrupt mode is enabled. The flag remains active until a read operation transfers the data and resets the reference data register and the flag.

INSTALLATION REQUIREMENTS

The digital change of state is a single card for use in any station location of the computer interface unit or computer interface expander.

Input to the digital change of state from external contact pairs or logic levels is via the connector at the computer interface unit/computer interface expander backplane.

POWER REQUIREMENTS

Logic power of +5v is supplied by the computer interface unit/computer interface expander module.

CABLING AND CONNECTORS

External signals are through a customer-furnished cable assembly connected to the computer interface unit/computer interface expander module at the digital change-of-state station location.

The following connector hardware is supplied with each unit:

- Connector shell, CDC part no. 39498600
- Connector block, CDC part no. 94261810
- Contacts, CDC part no. 94245600

A Berg Electronics, Incorporated, crimp tool (No. HT66) is required for crimping contacts to the customer-furnished cable.

A ground bale is used between pins B18 and B31 for input common soldered connections.

INTERFACE CHARACTERISTICS

DATA/CONTROL BUS INTERFACE

The data/control interface between the computer interface unit/computer interface expander module and station devices such as the digital change of state is described in the Computer Interface Unit/Computer Interface Expander Hardware Reference/Maintenance Manual.

EXTERNAL I/O INTERFACE

Pin assignments for interfacing an external device to the digital change of state are given in table 3-1.

The external inputs are:

- Logic level inputs

  False = 0 to +0.4 vdc at 1.6 milliamperes
  True = +2.4 to +5.25 vdc

- Contact pairs

  False = Closed contact pair
  True = Open contact pair

  Contact current is approximately 1.6 milliamperes.

  One side of all input pairs connects to system ground.

COOLING REQUIREMENTS

The digital change of state has no special cooling requirements. Standard blower cooling provided to the computer interface unit/computer interface expander is adequate. (See table 1-2 of the Computer Interface Unit/Computer Interface Expander Hardware Reference/Maintenance Manual.)

ENVIRONMENTAL REQUIREMENTS

For environmental requirements, see the Computer Interface Unit/Computer Interface Expander Hardware Reference/Maintenance Manual.

PREPARATION FOR USE

Set the delay jumper and the adjustment potentiometer for signal conditioning delay suitable to the particular application.

TABLE 3-1. EXTERNAL INTERFACE

Pin No.	Signal	Description
A18	–	
B18	GND	Ground
A19	INB00	Input data bit 00
B19	INB01	Input data bit 01
A20	INB02	Input data bit 02
B20	INB03	Input data bit 03
A21	INB04	Input data bit 04
B21	INB05	Input data bit 05
A22	INB06	Input data bit 06
B22	INB07	Input data bit 07
A23	INB08	Input data bit 08
B23	INB09	Input data bit 09
A24	INB10	Input data bit 10
B24	INB11	Input data bit 11
A25	INB12	Input data bit 12
B25	INB13	Input data bit 13
A26	INB14	Input data bit 14
B26	INB15	Input data bit 15
A27	–	
B27	–	
A28		
B28		
A29		
B29	–	
A30	–	
B30	–	
A31	–	
B31	GND	Ground

An introduction to the digital change-of-state theory of operation appears in section 1. A simplified logic is given in figure 5-1.

The digital change of state contains the signal conditioning required to interface to external contact closures or logic level inputs.

The unit is capable of inputting the external data to the central processing unit and of notifying the central processing unit (via interrupt) of any change in the external data with respect to the latest data input.

The significant circuit blocks are:

- Instruction decoding logic
- External input conditioning circuits
- Reference data register (16-bit)
- Comparator (16-bit)
- Signal conditioning delay (interrupt delay)

CIRCUIT DESCRIPTION

INSTRUCTION DECODING LOGIC

Refer to figure 5-2, sheet 1, for the instruction decoding logic. Computer interface unit/computer interface expander data/control bus inputs are:

- SSxxF (station select)
- WRITF (write)
- READF (read)
- FUSTF (function status or data)
- MCLR (master clear)

The decode logic develops the following signals:

- Station write function (false at TP05)

  The station write function provides clocking to the type D interrupt enable flip-flop. The clocked data to the flip-flop is from data bit 00. The interrupt enable flip-flop output is at TP03.

- Station read data (TP30)

  The station read data is used to update the data reference register and to enable the data transmitters for inputting data to the central processing unit.

- Station read data or master clear (false at TP07)

  This is used to reset the interrupt flip-flop, the interrupt delay one-shot, and the anti-retrigger latch.

- Station write function or read data (TP01)

  This generates the reply response from the DCOS.

EXTERNAL INPUT CONDITIONING CIRCUITS

For the external input conditioning circuits refer to figure 5-2, sheets 2 and 3.

The 16 external inputs are labeled INB00 through INB15.

Low-pass RC networks on each input bit reduce high frequency noise. Diode networks and DTL integrated circuits at the input provide reliable conversion of external inputs to TTL-compatible levels. These bit circuits connect to the reference data register and the comparator.

Test points for each input data are shown on the schematic.

DATA REFERENCE REGISTER

The data reference register is shown in figure 5-2, sheets 2 and 3.

The 16-bit data register consists of four 74175-type integrated circuits. These load the external input word at the leading edge of a station read data signal. This same word is transmitted to the central processing unit via the computer interface unit/computer interface expander data control bus as DB00F through DB15F.

16-BIT COMPARATOR

The 16-bit comparator is shown in figure 5-2, sheets 2 and 3.

The comparator consists of four 7485-type integrated circuits. The external inputs are constantly compared to the data reference word. The EQL signal (TP27) is high when the words are equal. Any state change of the external inputs results in EQL (comparator output) going low. This state change initiates a delay at completion of the delay interval; the interrupt flag flip-flop is set.

Test points are shown for each four bits of the comparator.

SIGNAL CONDITIONING DELAY

Refer to figure 5-2, sheet 1, for the signal conditioning delay.

This circuit consists of a 74123-type oneshot and a latch formed by two inverters from a 7403 integrated circuit. The latch prevents the one-shot from being retriggered from state changes such as those resulting from contact bounce.

The delay allows time for contact bounce to die out and the input to reach a steady state before the interrupt signaling the state change is generated.

The central processing unit acknowledges the interrupt with a read data instruction. The delay allows the corresponding data input to be the new steady state.

Without the delay, a chain of interrupts and reads might result from contact bounce at the input. This could last for several milliseconds and waste central processing unit time.

The delay interval is set by the nut and bolt jumper and the potentiometer. The interval is adjusted to exceed the contact bounce interval anticipated with the particular external inputs used.

The first state change following a read instruction always generates an interrupt when the interrupt enable flip-flop is enabled. The interrupt occurs at the completion of the chosen delay interval regardless of further state changes occurring during the delay.

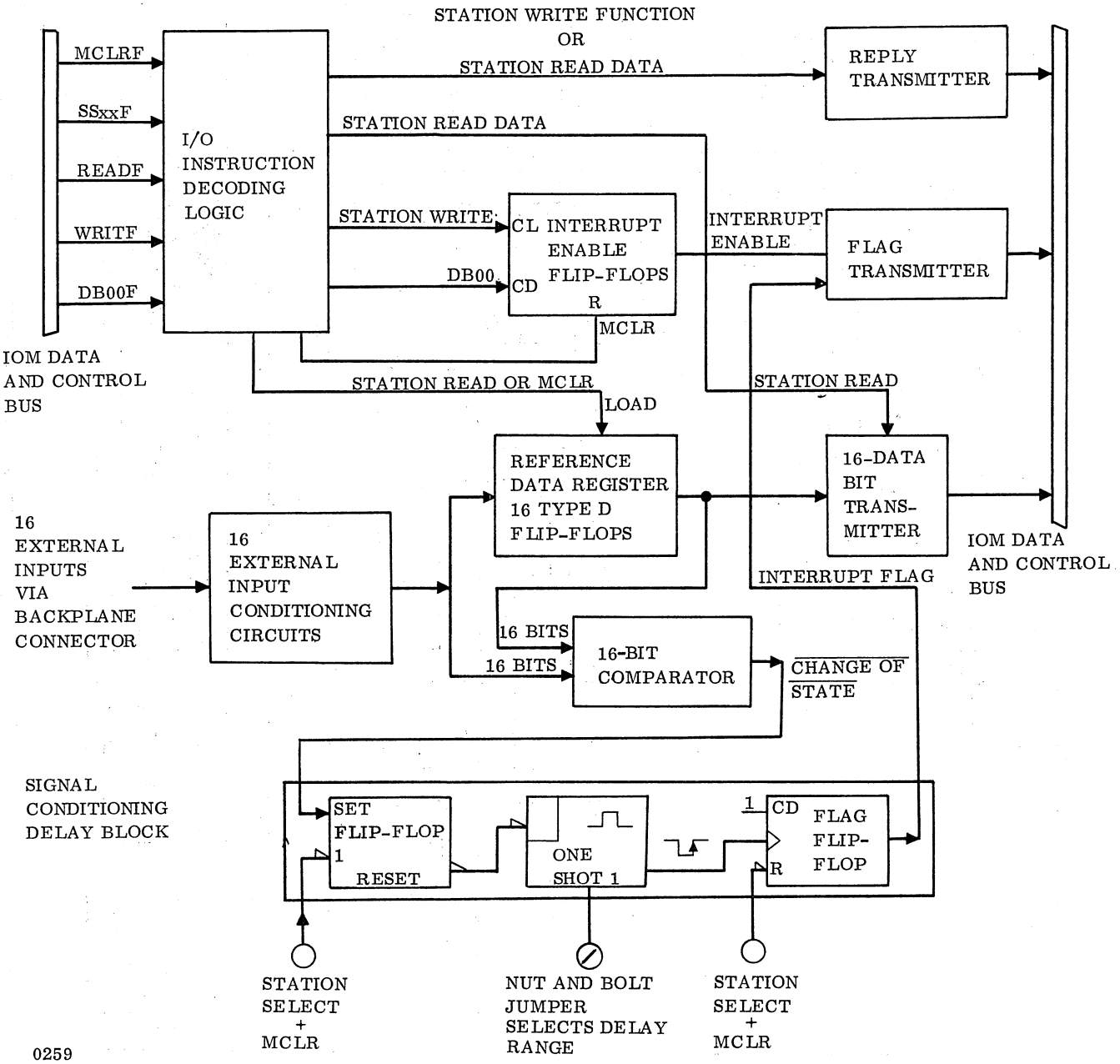


Figure 5-1. Digital Input Change-of-State Unit Simplified Logic Diagram

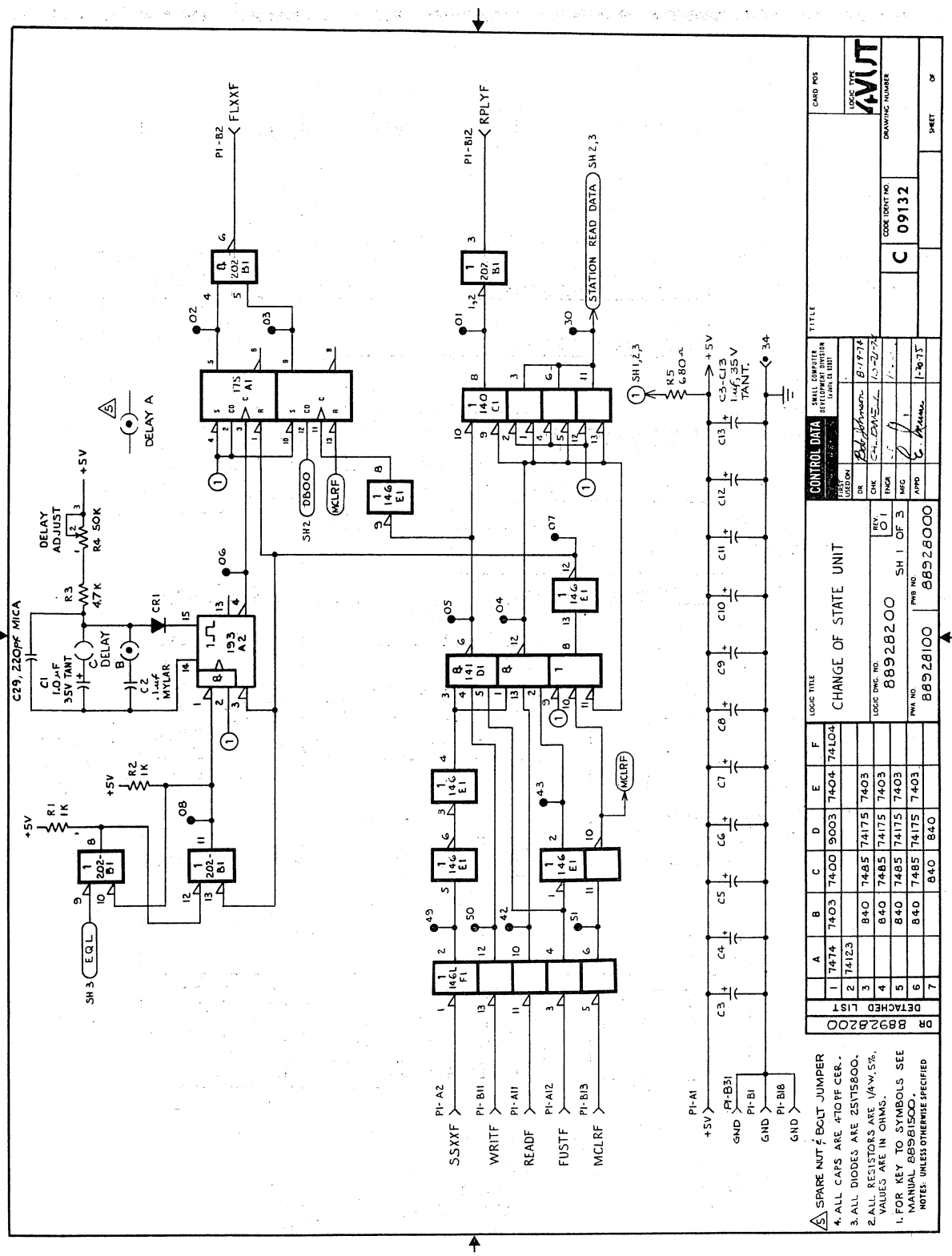


Figure 5-2. Digital Change-of-State Logic Drawing (Sheet 1 of 3)

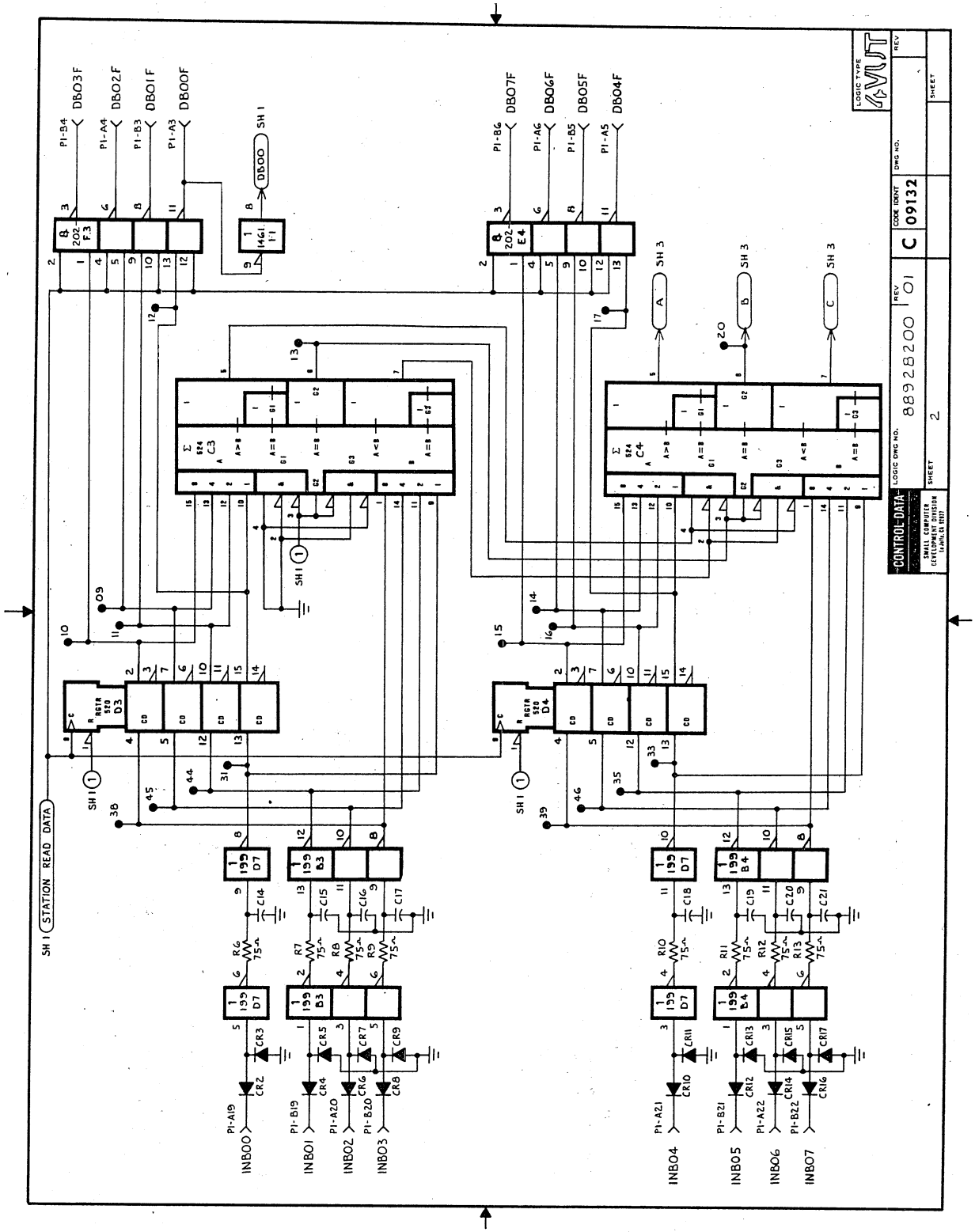


Figure 5-2. Digital Change-of-State Logic Drawing (Sheet 2 of 3)

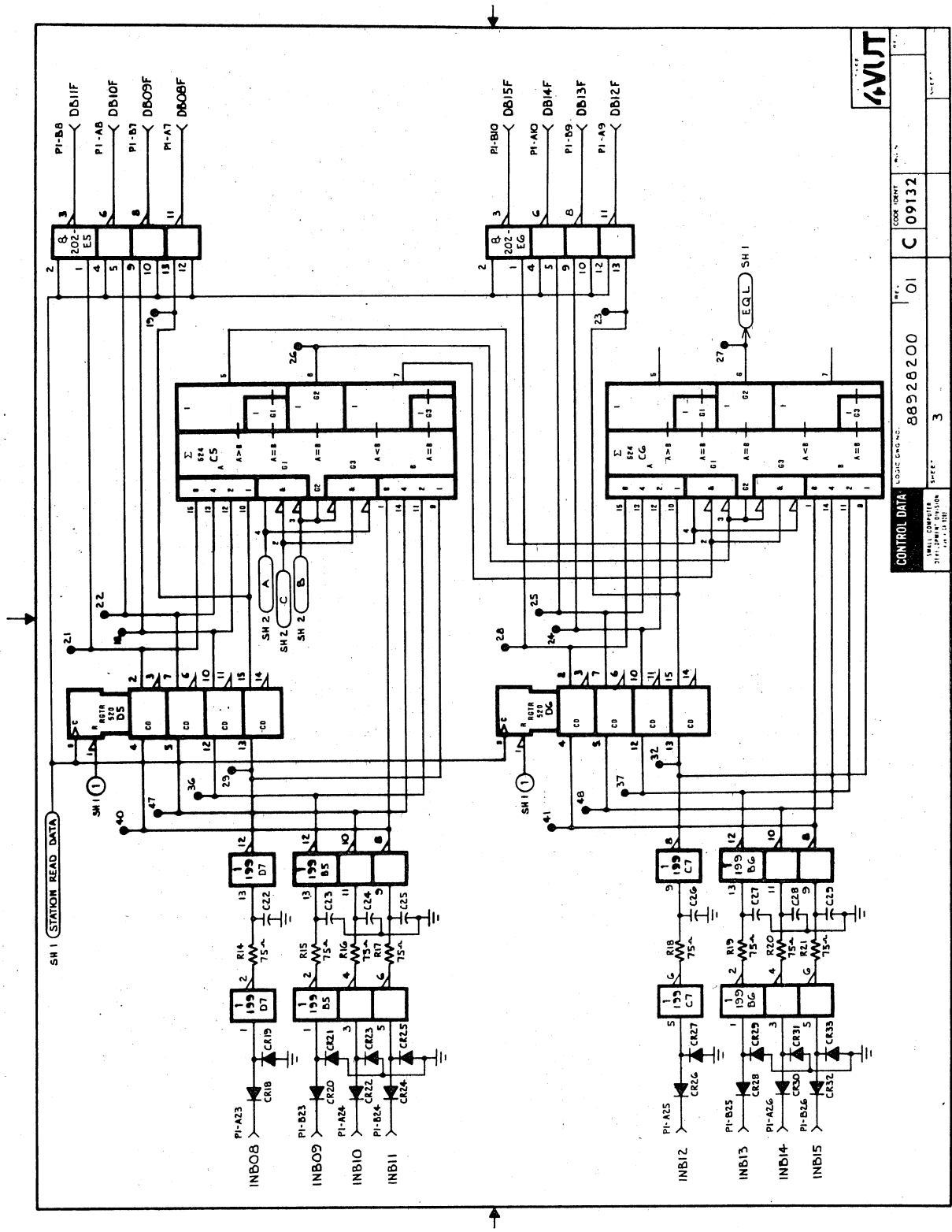


Figure 5-2. Digital Change-of-State Logic Drawing (Sheet 3 of 3)

PREVENTIVE MAINTENANCE

Check the delay time at six-month intervals.

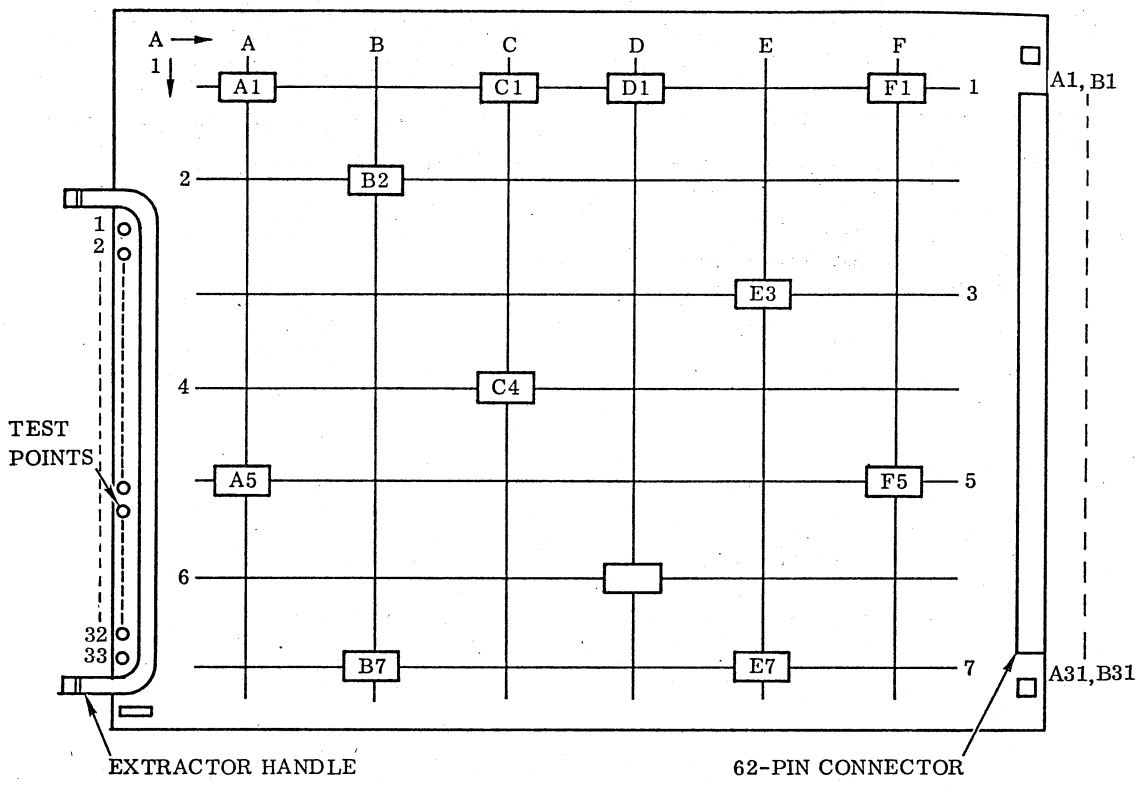
TROUBLESHOOTING

Troubleshooting is conveniently performed by connecting the digital change of state to a 1553 Digital Output Unit.

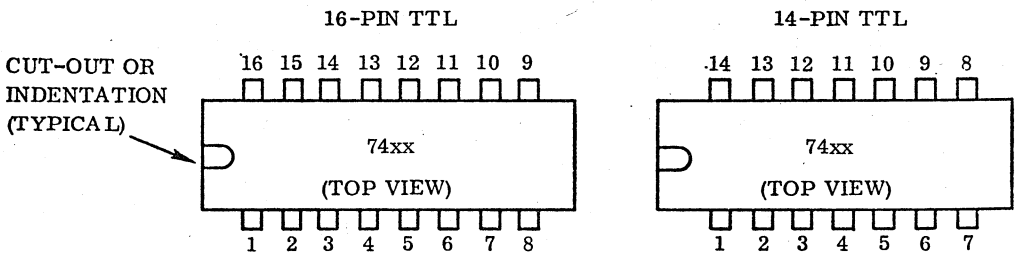
Contact bounce may be simulated by a series of outputs to the 1553 to allow given bits to repeatedly change and return to normal over an appropriate interval.

MAINTENANCE AIDS

- 2NMT card extender no. 39844100
- Digital output unit (DOU), part no. 39842500
- Standard pin and chip locations (figure 6-1)
- Key to Logic Symbols



PRINTED WIRING BOARD (PWB) COMPONENT SIDE CHIP LOCATION



PIN CONFIGURATION, TOP VIEW

095

Figure 6-1. Board Component and Pin Location

This section contains the printed wiring assembly (figure 7-1) and parts list for the digital change-of-state unit.

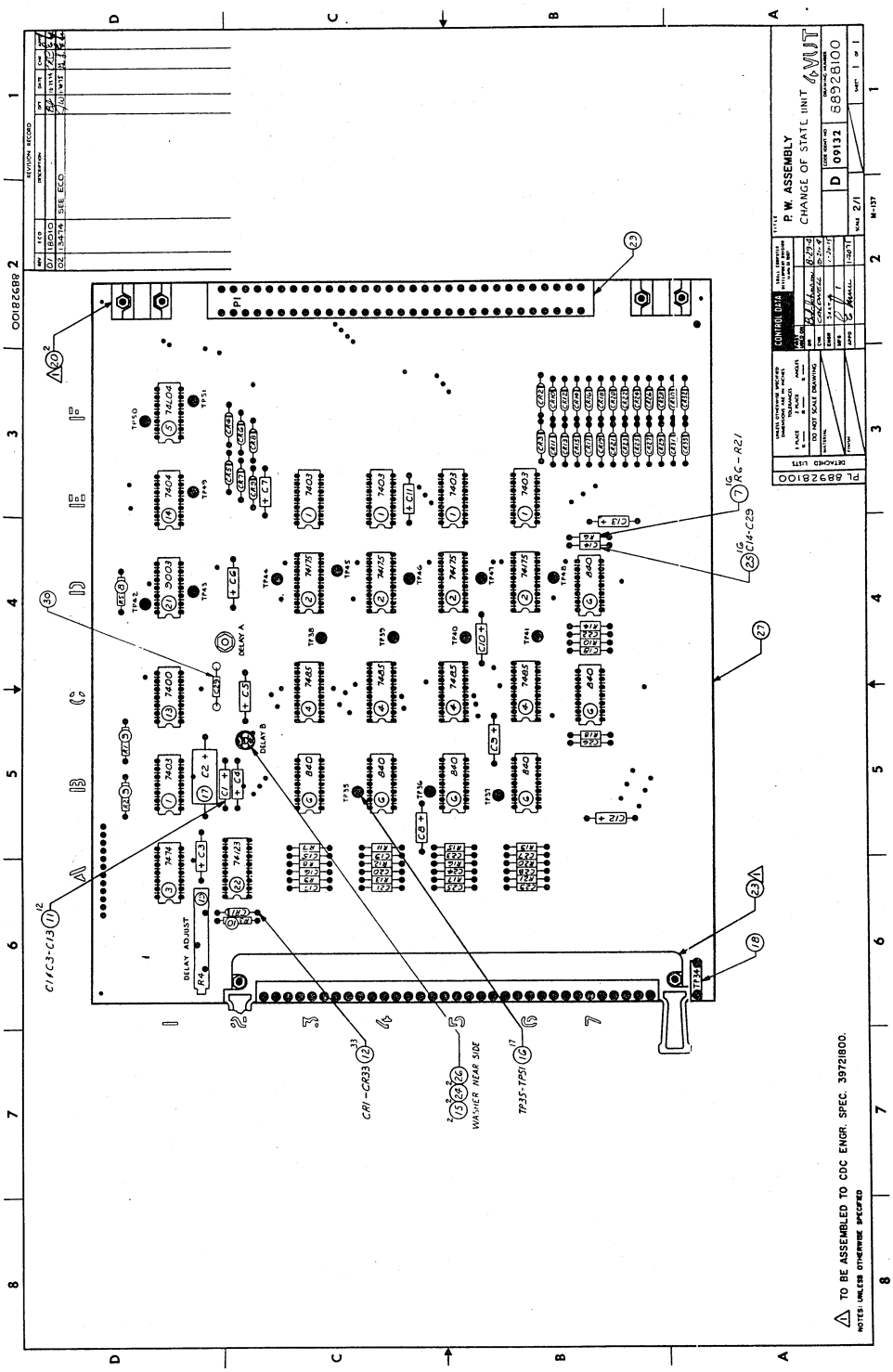


Figure 7-1. Change-of-State Unit Printed Wiring Assembly

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
88928100	02	C I B	D	PWA-CHANGE OF STATE UNIT 4VUT	DS	IOM	10/15/74	

PR

PROCESSING DATE	PAGE NUMBER
01/15/75	~~1/ 1~~

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
1	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
2	A	15104500	400	PC	ACCEPT TEST TYPE 74175	IN					PPP4		N
3	A	15104800	100	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP4		N
4	A	15108600	400	PC	I.C.4BIT COMPARATOR 7485	IN					PPP4		N
5	H	15112700	100	PC	INT CKT 74L04	IN					PPP4		N
6	H	15112800	600	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
7	C	24500036	1400	PC	RES FXD .25W 75 OHMS	IN					PPP4		N
8	C	24500059	100	PC	RES FXD .25W 680 OHMS	IN					PPP4		N
9	C	24500063	200	PC	RES FXD .25W 1000 OHMS	IN					PPP4		N
10	C	24500079	100	PC	RES FXD .25W 4700 OHMS	IN	013474	111874			PPP4		N
11	C	24505229	1200	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN					PPP4		N
12	A	25175800	3300	PC	DIODE(1N914)	IN					PPP4		N
13	A	36186800	100	PC	INT CKT 7400 TTL QUAD 2 INPUT	IN					PPP4		N
14	A	36187100	100	PC	INT CKT 7404 TTL HEX INVERTER	IN					PPP4		N
15	A	38A37923	200	PC	SCREW,NYLON,4-40-5/16,RH	IN	013474	111874					N
16	A	38A38005	1700	PC	TERM,TUR-SUBMIN,TIN DIP .062	IN					PPP4		N
17	A	38956724	100	PC	CAP,MYLAR+FOIL .1 MFD	IN	013474	111874					N
18	A	38958502	100	PC	TEST JACK, BLACK	IN					PPP4		N
19	A	38963811	100	PC	POT, TRIM, 50K OHMS	IN	013474	111874					N
20	C	39427500	200	PC	GUIDE,APPROACH	IN					PPP4		N
21	A	50250700	100	PC	IC TTL TRPL 3 INPUT NAND 9003	IN					PPP4		N
22	C	50254300	100	PC	IC TTL2 OR MV-A 74123	IN					PPP4		N
23	C	52436000	100	PC	AIR SEAL - 25 PAK	IN					PPP4		N
24	A	84553301	200	PC	NUT,NYLON,4-40	IN	013474	111874					N
30	A	84996717	100	PC	CAP,CER 100V 220 PF	IN	013474	111874			PPP4		N
25	A	84996721	1600	PC	CAP,CER 100V 470 PF	IN					PPP4		N
26	F	88774301	200	PC	LOCK WASHER INT TOOTH NO. 4	IN	013474	111874					N
27	C	88928000	100	PC	PWB-CHANGE OF STATE UNIT	IN					PPP4		N
28	C	88928200	REF	PC	LOGIC DIAGRAM 4VUT	IN							N
29	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N

NUMBER OF LINE ITEMS = 30
HIGHEST FIND NUMBER = 30

PROJECT ENGINEER
DON SEXTON

AA 2709 REV. 2-73

RECYCLE FOR THE FUTURE

COMMENT SHEET

MANUAL TITLE CDC® DK617-A Change of State Unit Hardware Maintenance Manual

PUBLICATION NO. 96767760 REVISION B

FROM NAME:

BUSINESS ADDRESS:

COMMENTS: This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number to which your comment applies.

CUT ALONG LINE

STAPLE

STAPLE

FOLD

FIRST CLASS
PERMIT NO. 333

LA JOLLA, CA.

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
PUBLICATIONS AND GRAPHICS DIVISION
4455 EASTGATE MALL
LA JOLLA, CALIFORNIA 92037

CUT ALONG LINE

FOLD

STAPLE

STAPLE